REMARKS

Amendments to Claims 17 and 18.

Claims 17 and 18 have been amended to correct a typographical error. Claim 18 was mistakenly identified as claim 17 in the last Response to Office Action.

Rejection of Claim 1 Under 35 U.S.C. §103(a), *Hsue* (5,378,654) in view of *Chang et al* (5,893,740).

The invention of claim 1 includes a method of forming a contact hole that is self-aligned with a transistor gate having a gate length of less than 0.2 μm. Further, the contact hole can be formed without an etch stop liner for a contact hole etch. This is in contrast to conventional approaches that include an etch stop liner, or form contacts on products having gate lengths of 0.2 μm or greater.

As was noted in the previous Response to Office Action, dated December 22, 2000, conventional approaches to contacts of 0.2 μm and less, have included etch stop layers to avoid unwanted etch results.[1] The present invention is believed to differ from the prior art and conventional approaches in that a contact hole may be formed without an etch stop liner, where such a contact hole is self-aligned with respect to a transistor gate having a length less than 0.2 μm. The cited references, *Hsue* in view of *Chang et al.*, do not suggest such an invention.

Due to differences in the technologies described in *Hsue* and *Chang et al.*, it is not believed that it would be obvious to combine the references. *Hsue* teaches a self-aligned contact process, while *Chang et al.* shows the formation of a transistor having a gate length that is typically 0.1 μm. However, substantial differences in scale exist between the two references. *Hsue* appears directed toward conventionally large scale geometries. In particular, the disclosed embodiment of *Hsue* appears to show a self-aligned contact process for a gate length of 0.8 μm – nearly four times the size limit of the claimed

[1] See the Specification, Page 5, Line 24. See also Page 8, Lines 17-20 for general protective properties of an etch stop (i.e., a liner). See Appendix A for the reference *Jeng et al.* (U.S. Patent No. 6,033,962) which repeats the conventional belief that protective

invention.[2] It appears apparent that *Hsue* is concerned with relatively large size transistor gate lengths.

In contrast, a transistor according to *Chang et al.* can have a gate length of 0.1 μm or less. However, such a transistor is a short channel transistor having specific structures and requirements for proper operation. As noted in *Chang et al.*, short channel transistors may include many serious problems.[3] It is believed that these particulars argue against combination with the approach of *Hsue*, which concerns large gate lengths.

In addition, it is stressed that *Hsue* remains silent with respect to key elements of *Chang et al.*, and vice versa. For these reasons, it is not believed that the cited combination provides a suggestion, desirability or reasonable potential for success required for an obviousness rejection.

As noted above, *Hsue* is entirely silent with respect to the formation a structure having a gate length of less than 0.2 μm. All descriptions appear aimed at gate lengths of about 0.8 μm. Therefore, it is not believed that the reference provides any indication that the described process would work for gate lengths less than 0.2 μm without an etch stop. At the same time, *Chang et al.* is completely silent with respect to the formation contacts. Thus, it is not believed that *Chang et al.* provides indication that a self-aligned contact without an etch stop would work for structure having gate lengths of less than 0.2 μm.

Accordingly, because the invention of claim 1 includes limitations not present in, or suggested by the cited combination of references, the rejection of claim 1 is traversed.

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liners are needed for sub-micron feature sizes. In particular, see *Jeng et al.*, Col. 2, Lines 1-5.

[2] See *Hsue*, FIGS. 2A and 2B, and accompanying descriptions in Col. 3 and 4. In particular, Col. 3, Lines 65-67 indicate a polysilicon/polycide layer **42** has a thickness of about 3,000 Å. A silicon dioxide layer **46** has a thickness of about 2,500 Å. FIGS. 2A and 2B thus appear to be drawn close to scale. A measurement of the gate length in FIGS. 2A and 2B yields a length of about 8,000 Å, which equals 0.8 μm. Applicant's claim 1 limitations recite a gate of length less than 0.2 μm.

[3] See *Chang et al.*, Col. 1, Lines 10-19 describing the presence of short channel effects generally, and the serious problem of punchthrough in particular.

Rejection of Claims 2-11 Under 35 U.S.C. §103(a), *Hsue* (5,378,654) in view of *Chang et al.*(5,893,740), and further in view of *Nulty et al.* (5,468,342).

To the extent that this rejection relies on the combination of *Hsue* in view of *Chang et al.*, the arguments set forth for claim 1 are incorporated by reference herein.

It is initially noted that *Nulty et al.* presents a conventional approach that includes an etch stop liner.[4] Therefore, at best, *Nulty et al.* fails to distinguish between approaches that include etch stop liners and those that do not include etch stop liners. Because *Nulty et al.*, only shows examples of methods that include an etch stop liner, it is not believed that it would have been obvious combine the teachings of *Nulty et al.* with the large geometry no-liner method of *Hsue* or the method of *Chang et al.*, which provides no etch teachings at all.

Other claims have further limitations that are distinguishable from the references. With respect to claim 3, the invention of claim 3 further includes reactive plasma etching through an insulating layer comprising doped silicon dioxide, where a phosphorous doping concentration is greater than 5% by weight. Because the cited references are silent as to this particular level of doping concentration, it is believed that this rejection is unsustainable.

Hsue appears to teach away from claim 3, as all examples show a contact hole through apparently undoped silicon dioxide.[5] *Chang et al.* appears to be concerned only with the formation of the particular short channel transistor, and has no teachings regarding an insulating layer formed over such a device. *Nulty et al.* refers to oxide layers that may be doped with boron, phosphorous or both.[6] However, particular concentrations are not discussed. As noted in the Specification, phosphorous concentrations over 5% can have undesirable effects. In light of this, and the fact that the

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[4] See *Nulty et al.*, Fig. 4 and Col. 3, Lines 50-51, describing etch stop layer 403. See also, Figs. 12-14 and Col. 10, Lines 42-49, which discuss etch stop layer 1203, and Figs. 15-17, which show an etch stop layer 1503.

[5] See *Hsue*, Col. 2, Lines 3-5 and Col. 4, Lines 19-22, which describe silicon dioxide layers **21** and **46**, with no indication of doping.

[6] See *Nulty et al.*, Col. 1, Lines 17-25.

cited references do not teach the claimed phosphorous dopant concentration, it is believed that claim 3 is patentable over the cited combination of references.

In light of all the above arguments, it is believed that the rejection of claims 2-11 is traversed.

Rejection of Claim 12 Under 35 U.S.C. §103(a), *Hsue* (5,378,654) in view of *Chang et al.* (5,893,740).

The invention of claim 12 includes etching a contact hole through a first insulating layer of doped silicon dioxide. Two etch selectivity limitations are recited. A first selectivity is between the first insulating layer and the sidewall, and is greater than ten to one. A second selectivity is between the first insulating layer and the substrate, and is greater than one hundred to one. As noted in the Specification, by etching a first insulating layer with such selectivities between a sidewall and substrate, it may be possible to dispense with the need for a protective liner that is typically used in conventional approaches.[7]

Because the cited combination of references does not disclose or suggest all elements of the claimed invention, it is believed that the rejection of claim 12 is unsustainable.

Neither reference discloses an etch selectivity between a sidewall and a first insulating layer that is greater than ten to one. The example of *Hsue* shows a contact hole that is etched through a deposited layer made from the same material as a sidewall.[8] Thus, there would appear that *Hsue* teaches no etch selectivity between an insulating layer and sidewall (an etch selectivity of 1:1). It is not understood how an absence of etch selectivity can suggest the very particular etch selectivity recited in claim 12.

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[7] See the Specification, Page 25, Lines 8-11 and Lines 18-20.

[8] See *Hsue*, FIG. 1C and description at Col. 1, Lines 54 to 66, which describe the formation of a spacer **18** from a layer of CVD silicon dioxide. See also FIG. 1D and description at Col. 2, Lines 3-8, which indicates layer **21** is also CVD silicon dioxide.

As noted above, the other reference *Chang et al.* provides no teachings regarding insulating layers and/or contact hole formation. Therefore, any motivation or suggestion for a particular etch selectivity is lacking in *Chang et al.*

In the absence of any teachings of selectivity in the cited art, or motivation to change etch selectivity, it is believed the particular etch selectivity limitation of greater than 10:1 and greater than 100:1, as recited in claim 12, are obvious only with the benefit of impermissible hindsight.

Such a similar absence of teachings or suggestion for modification exists with respect to a first insulating layer comprising doped silicon dioxide. As noted above, *Hsue* teaches an insulating layer of only undoped silicon dioxide. Because the reference only teaches undoped silicon dioxide insulating layers, at best, *Hsue* provides no motivation for including a doped silicon dioxide, and at worst teaches away from Applicant's invention. With respect to *Chang et al.*, this reference does not even show an insulating layer containing a contact hole. Because the references do not show a doped silicon dioxide insulating layer, and there is no express or implied suggestion for such a modification, it is believed that this ground for rejection is improper and should be withdrawn.

For all of these reasons, the rejection of claim 12 is respectfully traversed.

Rejection of Claims 18 and 19 Under 35 U.S.C. §103(a), *Hsue* (5,378,654) in view of *Chang et al.* (5,893,740), further in view of *Avanzino et al.* (5,776,834).

The invention of claim 18 includes a method of forming a hard mask of substantially undoped silicate glass over an insulating layer comprising doped silicon dioxide. Such a hard mask may have openings at a contact hole location. A contact hole is formed at the contact hole location through the insulating layer. The contact hole is also formed between conducting structures separated from one another by less than 0.4 microns. It is believed that such an arrangement can be considered contrary to the approaches of the cited art, as a hard mask and underlying insulating material may both

include silicon dioxide. The cited art does not appear to teach an etch that may distinguish between two layers that both include silicon dioxide.

To the extent that this rejection relies on the combination of *Hsue* in view of *Chang et al.*, the arguments set forth for claim 1 are incorporated by reference herein. Namely, *Hsue* concerns large geometry devices, while *Chang et al.* concerns, different, small short channel devices.

A similar difference between *Hsue* and *Avanzino et al.* is believed to exist. Like *Chang et al.*, *Avanzino et al.* is entirely silent regarding the formation of contact holes. In fact, *Avanzino et al.* teaches the exact opposite of forming contact holes -- filling spaces between conductive lines.[2] Because *Avanzino et al.* concerns filling spaces, the structures do not even include sidewalls as recited in claim 18. For this reason, it is believed that no motivation exists for combining *Avanzino et al.* and *Hsue*, as one addresses opening a contact hole in an insulating while the other concerns filling spaces with an insulating layer. In addition, a self-aligned contact method according to *Hsue* is not possible with a non-sidewall structure, such as that shown in *Avanzino et al.*

It is argued in the Office Action that a hard etch mask of undoped silicate glass in conjunction with a doped silicon dioxide insulating layer would be obvious to one skilled in the art. It is noted that the invention of claim 18 incorporates such a hard mask in a method with further limitations. As noted above, such limitations include conducting structures with sidewalls separated from one another by less than 0.4 microns, and forming a contact hole without a protective liner. None of the references indicates why or how motivation for incorporating such a hard etch mask in combination with these particular features is desirable, or has a reasonable expectation of success.

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[2] See *Avanzino et al.*, Col. 1, Lines 18-22, which indicate the invention relates to forming an insulating layer on and between metal conductive lines. See also, *Avanzino et al.*, Col. 5, Lines 7-9, which describes a method that simultaneously deposits and etches a material to fill a gap without small voids.

In light of the fact that none of the references show a hard etch mask[10], it is believed the only suggestion for including an undoped silicate glass hard etch mask exists in Applicant's disclosure, and thus is arrived at through hindsight.

For all the reasons noted above, the rejection of claims 18 and 19 is believed to be improper and should be withdrawn.

Claim 17 and 18 have been amended to correct typographical errors in the previous Office Action. The present claims 1-14 and 16-19 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

6/14/01

Bradley T. Sako
Reg. No. 37,923

Bradley T. Sako
Attorney/Agent
3954 Loch Lomand Way
Livermore, CA 94550
Tel. 1-408-839-1082
Fax 1-925-961-0184

[10] See *Hsue* FIGS. 1D and 2B, which show conventional etch masks of photoresist 22 and 52. See *Chang et al.* and *Avanzino et al.*, which show no contact etch masks whatsoever.

Amendments with Markings to Show Proposed Changes.

Please substitute claim 17 with the following.

17. (Twice Amended) **[A method, comprising]** **The method of claim 16, wherein**:

the hard etch mask comprises silicon dioxide; and

the first insulating layer comprises phosphorous doped silicon dioxide

[forming a hard mask comprising substantially undoped silicate glass over an insulating layer comprising doped silicon dioxide, the hard mask having openings over a contact hole location; and

forming a contact hole at the contact hole location through the insulating layer between conducting structures separated from one another by less than 0.4 microns and having sidewalls, without forming a protective liner over the conducting structures].

Please substitute claim 18 with the following.

18. (Amended) A method, comprising:

forming a hard mask comprising substantially undoped silicate glass over an insulating layer comprising doped silicon dioxide, the hard mask having openings over a contact hole location; and

forming a contact hole **at the contact hole location** through **[an]** **the** insulating layer between conducting structures separated from one another by less than 0.4 microns and having sidewalls, without forming a protective liner over the conducting structures**[, wherein the insulating layer comprises silicon dioxide]**.

APPENDIX A

U.S. Patent No. 6,033,962, *Jeng et al.*